

SENSITIVITIES ANALYSIS OF THE CURRENT MIRRORS WITH MOS-FET FOR THE BASIC FUZZY LOGIC GATES/CIRCUITS

Emil SOFRON
University of Pitesti
emil.sofron@upit.ro

Keywords: current sources and mirrors, fuzzy logic gates/circuits, bounded-difference, sensitivities, SPICE simulation

Abstract: *The paper presents a comprehensive approach of the fuzzy logic gates/circuits from both technological and circuit analysis standpoint, using SPICE simulation, based on computing the sensitivities of current mirrors with n and p -channel MOS-FET (using units or tens microns for L and W parameters). CMOS technology has been recognized as the technology for implementing fuzzy logic gates/circuits in the current mode, which offers a high versatility for different fuzzy logic operations, low power dissipation and high integration density. The basic units of fuzzy logic gates/circuits are the current mirrors with single and/or multiple outputs, usually designed and fabricated in 5-10 microns CMOS technology.*

1. INTRODUCTION

The properties of the MOS-FET transistor (with small-area) make it highly attractive for some types of VLSI fuzzy logic gates/circuits and systems [1], which are based on the current sources/mirrors with certain advantages.

In this paper are considered the fuzzy logic gates/circuits with current sources and/or mirrors, for which are considered the following aspects:

- the topology of circuit;
- the operating mode (in current or in voltage);
- the basic units to be used.

In fact, the topologies of the fuzzy logic gates/circuits [2] don't differ essentially from the topologies corresponding of the crisp logic gates/circuits [3], but the inputs and outputs are fuzzy quantities and the characteristic functions are the fuzzy mappings [4].

The first part of the paper presents the basic elements of the fuzzy logic gate/circuit in a current mirror configuration using MOS/CMOS technology [5].

The second part of the paper presents results with SPICE simulations for a fuzzy logic

gate/circuit based on the $n(p)$ – MOS-FET current mirrors, using the different models of work (.DC, .TRAN and .AC models).

2. SENSITIVITIES ANALYSIS OF THE CURRENT MIRRORS WITH MOS - FET

In this part we present of the sensitivities for two the MOS-FET current sources/mirrors configurations (as in fig. 1 a, b), to which of the following parameters are considered:

W ($W_{1n, 2n, 1p, 2p}$) – width of the channel for $n(p)$ – MOS-FET transistors used;

L ($L_{1n, 2n, 1p, 2p}$) – length of the channel for $n(p)$ – MOS-FET transistors used;

k ($k_{1n, 2n, 1p, 2p}$) – gain coefficient (the process transconductance) for the $n(p)$ – MOS-FET transistors used;

γ ($\gamma_{1n, 2n, 1p, 2p}$) – coefficient of body-bias for the $n(p)$ – MOS-FET transistors used;

V_{T0} ($V_{T0_{1n, 2n, 1p, 2p}}$) - threshold voltage for the $n(p)$ – MOS-FET transistors used;

V_{DD} – voltage of bias for the $n(p)$ – MOS-FET transistors used.

Generally, the sensitivity for an electronic circuit is evaluated from two viewpoints: one is stability of the circuit operation and other is change continuity of the circuit's parameters, respectively. In this paper, the continuity is considered as the measure of evaluation of this change.

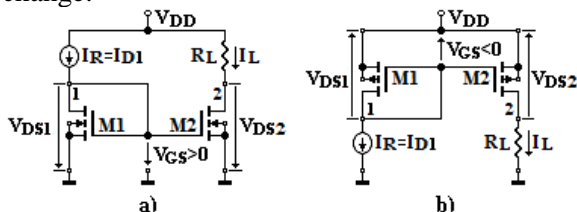


Fig. 1 – The basic current mirrors (with $V_{DD} = 10\text{ V}$ and $R_L = 500\text{ M}\Omega$):

- a/ with n – MOS-FET ($M_{1,n}: W_{1,n}, L_{1,n}, k_{1,n}, \gamma_{1,n}, VTO_{1,n}$ and $M_{2,n}: W_{2,n}, L_{2,n}, k_{2,n}, \gamma_{2,n}$),
to which $\Delta W_n = W_{2,n} - W_{1,n}$, $\Delta L_n = L_{2,n} - L_{1,n}$, $\Delta k_n = k_{2,n} - k_{1,n}$, $\Delta \gamma_n = \gamma_{2,n} - \gamma_{1,n}$, $\Delta VTO_n = VTO_{2,n} - VTO_{1,n}$;
- b/ with p – MOS-FET ($M_{1,p}: W_{1,p}, L_{1,p}, k_{1,p}, \gamma_{1,p}, VTO_{1,p}$ and $M_{2,p}: W_{2,p}, L_{2,p}, k_{2,p}, \gamma_{2,p}, VTO_{2,p}$),
to which $\Delta W_p = W_{2,p} - W_{1,p}$, $\Delta L_p = L_{2,p} - L_{1,p}$, $\Delta k_p = k_{2,p} - k_{1,p}$, $\Delta \gamma_p = \gamma_{2,p} - \gamma_{1,p}$, $\Delta VTO_p = VTO_{2,p} - VTO_{1,p}$.

To a $n(p)$ – MOS-FET, in saturation mode, any I_D (I_{D1} and I_{D2}) is sensitive to the change of W , L , k , γ , VTO and VDD parameters, for example:

$$I_D = \begin{cases} I_{D1} = k_{1,n(p)} \frac{W_{1,n(p)}}{L_{1,n(p)}} (V_{GS} - VTO_{1,n(p)})^2 = I_R \\ I_{D2} = k_{2,n(p)} \frac{W_{2,n(p)}}{L_{2,n(p)}} (V_{GS} - VTO_{2,n(p)})^2 = (k_{1,n(p)} + \Delta k_{n(p)}) \frac{W_{1,n(p)} + \Delta W_{n(p)}}{L_{1,n(p)} + \Delta L_{n(p)}} [V_{GS} - (VTO_{1,n(p)} + \Delta VTO_{n(p)})]^2 = \\ = k_{1,n(p)} \cdot \left(I + \frac{\Delta k_{n(p)}}{k_{1,n(p)}} \right) \cdot \frac{W_{1,n(p)}}{L_{1,n(p)}} \cdot \frac{I + \frac{\Delta W_{n(p)}}{W_{1,n(p)}}}{I + \frac{\Delta L_{n(p)}}{L_{1,n(p)}}} \left[V_{GS} - VTO_{1,n(p)} \left(I + \frac{\Delta VTO_{n(p)}}{VTO_{1,n(p)}} \right) \right]^2 = \\ = I_{D1} [I + e_{n(p)} (\Delta W_{n(p)}, \Delta L_{n(p)}, \Delta k_{n(p)}, \Delta \gamma_{n(p)}, \Delta VTO_{n(p)})] = I_L \end{cases}$$

where:

$$e_{n(p)} (\Delta W_{n(p)}, \Delta L_{n(p)}, \Delta k_{n(p)}, \Delta \gamma_{n(p)}, \Delta VTO_{n(p)})$$

is the effective error for any current source/mirror.

Next, we consider the global relative error e_g , which is defined through the relation:

$$e_g = \frac{\max |I_{D2}(m) - I_{D1}(m)|}{\max(I_{D2})} = \frac{\max |I_{D2}(m) - I_{D1}(m)|}{\max(I_{D1})}$$

where m can be any of the parameters: $W(W_{1,n(p)}, W_{2,n(p)})$, $L(L_{1,n(p)}, L_{2,n(p)})$, $k(k_{1,n(p)}, k_{2,n(p)})$, $\gamma(\gamma_{1,n(p)}, \gamma_{2,n(p)})$, $VTO(VTO_{1,n(p)}, VTO_{2,n(p)})$.

Particularly, a set of $W(W_{1,n(p)}, W_{2,n(p)})$, $L(L_{1,n(p)}, L_{2,n(p)})$, $k(k_{1,n(p)}, k_{2,n(p)})$, $\gamma(\gamma_{1,n(p)}, \gamma_{2,n(p)})$, $VTO(VTO_{1,n(p)}, VTO_{2,n(p)})$ parameters, satisfying the different operation condition, could be determined.

Practically, we define the partial differential sensitivity coefficient S is given by the following relation:

$$S_m^{I_{D2}} = \frac{m}{I_{D2}} \cdot \frac{\partial I_{D2}}{\partial m} \cong \frac{m}{I_{D2}} \cdot \frac{\Delta I_{D2}}{\Delta m}$$

where m is the parameter which was above mentioned.

Assuming that:

$$\frac{\Delta W}{W}, \frac{\Delta L}{L}, \frac{\Delta k}{k}, \frac{\Delta \gamma}{\gamma} \text{ and } \frac{\Delta VTO}{VT} \ll 1$$

results:

$$S_W^{I_{D2}} = \frac{W}{I_{D2}} \cdot \frac{\partial I_{D2}}{\partial W} \cong \frac{W}{I_{D2}} \cdot \frac{\Delta I_{D2}}{\Delta W}$$

$$S_L^{I_{D2}} = \frac{L}{I_{D2}} \cdot \frac{\partial I_{D2}}{\partial L} \cong \frac{L}{I_{D2}} \cdot \frac{\Delta I_{D2}}{\Delta L}$$

$$S_k^{I_{D2}} = \frac{k}{I_{D2}} \cdot \frac{\partial I_{D2}}{\partial k} \cong \frac{k}{I_{D2}} \cdot \frac{\Delta I_{D2}}{\Delta k}$$

$$S_\gamma^{I_{D2}} = \frac{\gamma}{I_{D2}} \cdot \frac{\partial I_{D2}}{\partial \gamma} \cong \frac{\gamma}{I_{D2}} \cdot \frac{\Delta I_{D2}}{\Delta \gamma}$$

$$S_{VTO}^{I_{D2}} = \frac{VTO}{I_{D2}} \cdot \frac{\partial I_{D2}}{\partial VTO} \cong \frac{VTO}{I_{D2}} \cdot \frac{\Delta I_{D2}}{\Delta VTO} = \frac{2}{I - \frac{V_{GS}}{VTO}}$$

With these current sources/mirrors, which were above analyzed for the evaluation of sensitivities to change parameters of $n(p)$ – MOS-FET device, different fuzzy logic gates could be implemented in MOS/CMOS technology [6]. For example, in this paper we discuss an elementary fuzzy logic gate (bounded

difference) in current-mode [7], which performs one of two basic logic operations:

$$\left\{ \begin{array}{l} \tilde{x} \quad t \quad \tilde{y} \Rightarrow \tilde{z} \\ V_{I1} \quad V_{I2} \quad V_2=R \cdot I_0 \\ \text{or} \\ \tilde{x} \quad t^* \quad \tilde{y} \Rightarrow \tilde{w} \\ V_{I1} \quad V_{I1} \quad V_2^*=R \cdot I_0^* \end{array} \right.$$

where t and t^* are the *norm*, *co-norm* operators, respectively.

Usually, in fuzzy logic gates/circuits, the *norm* is a operation of MIN (minimum), and the *co-norm* is a operation of MAX (maximum). For example, in fig. 2 is illustrated a basic CMOS fuzzy logic gate of MAX.

Because the diode D stops the reverse (or negative) current, the output current is the bounded-difference operation:

$$I_0 = \begin{cases} I_2 - I_1 & \text{if } I_2 \geq I_1 \\ 0 & \text{if } I_2 < I_1 \end{cases} \Rightarrow I_0 = \text{MAX}(0, I_2 - I_1)$$

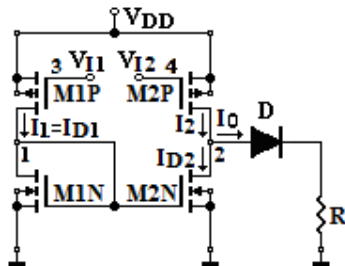


Fig. 2 – A CMOS fuzzy logic gate of MAX (cu VDD = 10 V and R = 100 kΩ → 20 kΩ).

In this circuit, the current mirror (with *MIN* and *M2N* devices) represents the main errors source. Usually, the drain currents have values ranging from tens to hundreds of micro-amperes. This formal analysis is completed by a computer simulation.

3. RESULTS OF SIMULATION AND DISCUSSION

In this part, we present the simulation results (using the SPICE) for the $n(p)$ – MOS-FET (fig. 1) and for the CMOS fuzzy logic gate of MAX (fig. 2), for example:

- to the current source/mirror with n – MOS-FET, for $W_{1,n} = 40\mu$ and $W_{2,n} = 10\mu$ (fig. 3);

- to the current source/mirror with p – MOS-FET, for $W_{1,p} = 50\mu$ and $W_{2,p} = 30\mu$ (fig. 4);

- to the current source/mirror with n – MOS-FET, for $W_{1,n} = k = 10, 15, 20, 25, 30, 35, 40$ and $W_{2,n} = 10\mu$ (fig. 5);

- to the current source/mirror with p – MOS-FET, for $W_{1,p} = k = 10, 20, 30, 40, 50$ and $W_{2,p} = 30\mu$ (fig. 6);

- to the current source/mirror with n – MOS-FET, for $L_{1,n} = k = 10, 15, 20, 25, 30, 35, 40$ and $L_{2,n} = 20\mu$ (fig. 7);

- to the current source/mirror with p – MOS-FET, for $L_{1,p} = k = 10, 15, 20, 25, 30, 35, 40$ and $L_{2,p} = 10\mu$ (fig. 8);

- to the current source/mirror with n – MOS-FET, for $k_{1,n} = 92.8E-6$ and $k_{2,n} = 72.8E-6$ (fig. 9);

- to the current source/mirror with p – MOS-FET, for $k_{1,p} = 57.6E-6$ and $k_{2,p} = 27.6E-6$ (fig. 10);

- to the current source/mirror with n – MOS-FET, for $k_{1,n} = 72.8E-6$ and $k_{2,n} = 92.8E-6$ (fig. 11);

- to the current source/mirror with p – MOS-FET, for $k_{1,p} = 27.6E-6$ and $k_{2,p} = 57.6E-6$ (fig. 12);

- to the current source/mirror with n – MOS-FET, for $k_{1,n} = KP_{1,n} = k$ (the parameter with following values: 72.8E-6, 82.8E-6, 92.8E-6, and 102.8E-6) and $k_{2,n} = 72.8E-6$ (fig. 13);

- to the current source/mirror with p – MOS-FET, for $k_{1,p} = KP_{1,p} = k$ (the parameter with following values: 27.6E-6, 37.6E-6, 47.6E-6, and 57.6E-6) and $k_{2,p} = 27.6E-6$ (fig. 14);

- to the current source/mirror with n – MOS-FET, for $\gamma_{1,n} = 0.764$ and $\gamma_{2,n} = 0.264$ (fig. 15);

- to the current source/mirror with p – MOS-FET, for $\gamma_{1,p} = 0.773$ and $\gamma_{2,p} = 0.373$ (fig. 16);

- to the current source/mirror with n – MOS-FET, for $V_{T0_{1,n}} = 0.705$ and $V_{T0_{2,n}} = 0.7$ (fig. 17);

- to the current source/mirror with p – MOS-FET, for $V_{T0_{1,p}} = -0.705$ and $V_{T0_{2,p}} = -0.7$ (fig. 18);

- to the CMOS fuzzy logic gate of MAX with $R = 20\text{ k}\Omega$ (fig. 19);

- to the CMOS fuzzy logic gate of MAX with $R = 20\text{ k}\Omega$ and $W = W_{1,n} = k = 10, 20, 30, 40$ (fig. 20);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $W=W_{1,p}= k = 30, 40, 50$ (fig. 21)

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $L=L_{1,n}= k = 10, 20, 30, 40$ (fig. 22);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $L=L_{1,p}= k = 10, 20, 30, 40$ (fig. 23);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $k=KP_{1,n}= k = 72.8\text{E-}6, 82.8\text{E-}6, 92.8\text{E-}6, 102.8\text{E-}6$ (fig. 24);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $k=KP_{1,p}= k = 27.6\text{E-}6, 37.6\text{E-}6, 47.6\text{E-}6, 57.6\text{E-}6$ (fig. 25);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $\gamma = \gamma_{1,n}= k = 0.264, 0.364, 0.464, 0.564$ (fig. 26);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $\gamma = \gamma_{1,p}= k = 0.373, 0.473, 0.573, 0.673$ (fig. 27);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $VT0 = VT0_{1,n}= k = 0.700, 0.701, 0.702, 0.703, 0.704, 0.705$ (fig. 28);

- to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $VT0 = VT0_{1,p}= k = -0.700, -0.701, -0.702, -0.703, -0.704, -0.705$ (fig. 29);

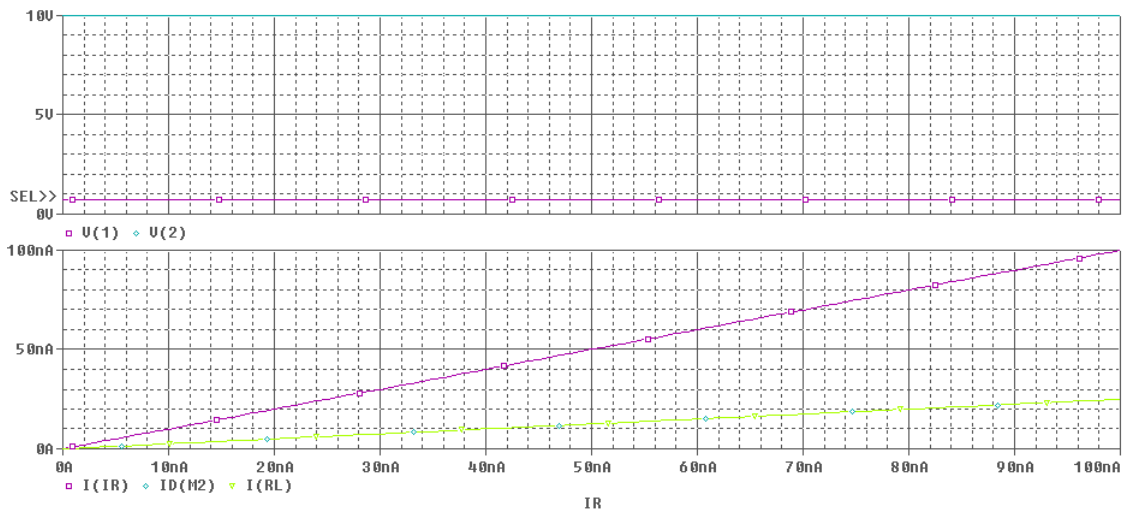


Fig. 3 – The results by simulation to the current source/mirror with n – MOS-FET, for $W_{1,n} = 40\mu$ and $W_{2,n} = 10\mu$.

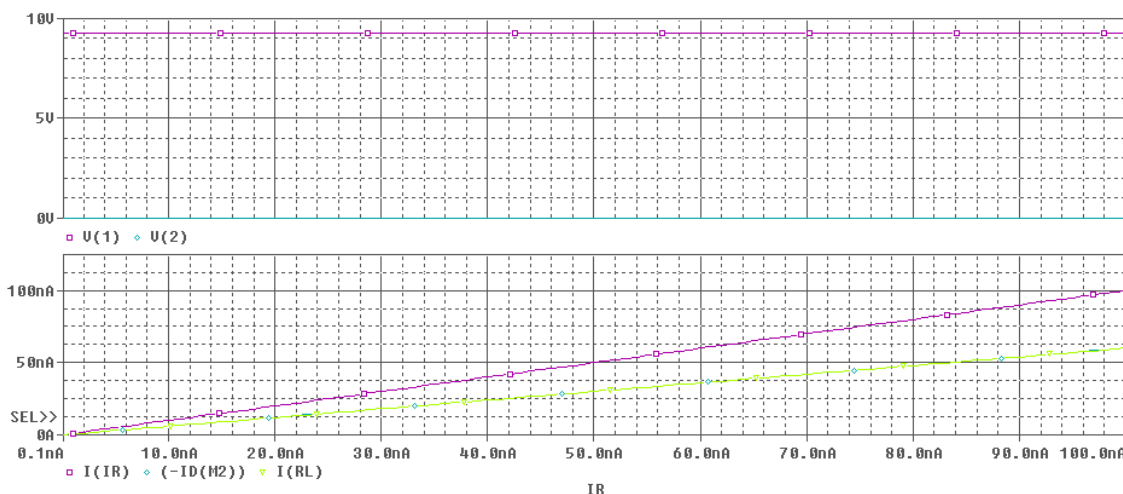


Fig. 4 – The results by simulation to the current source/mirror with p – MOS-FET, for $W_{1,p} = 50\mu$ and $W_{2,p} = 30\mu$.

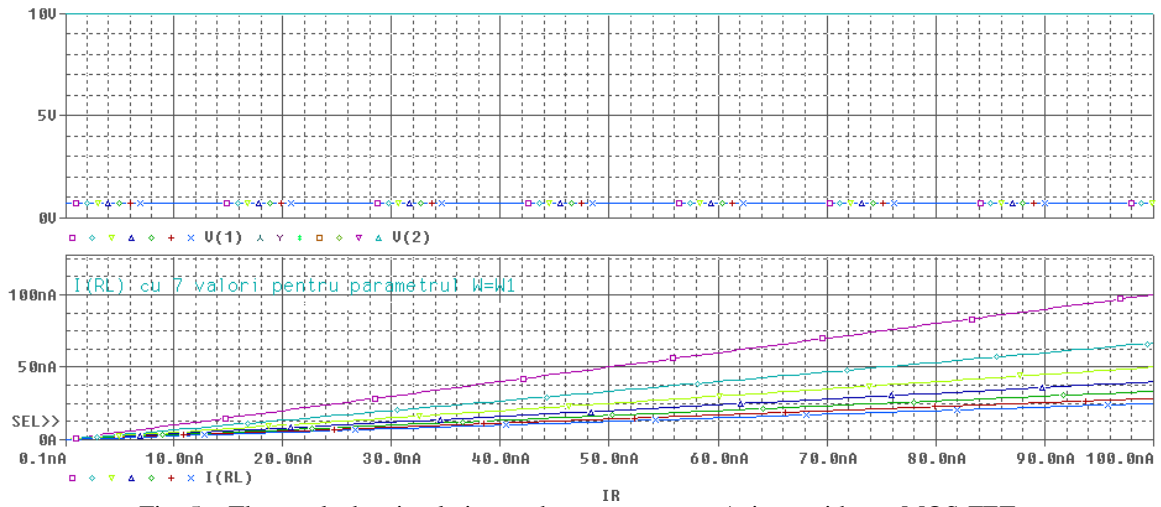


Fig. 5 – The results by simulation to the current source/mirror with n – MOS-FET, for $W_{1,n} = k = 10, 15, 20, 25, 30, 35, 40$ and $W_{2,n} = 10u$.

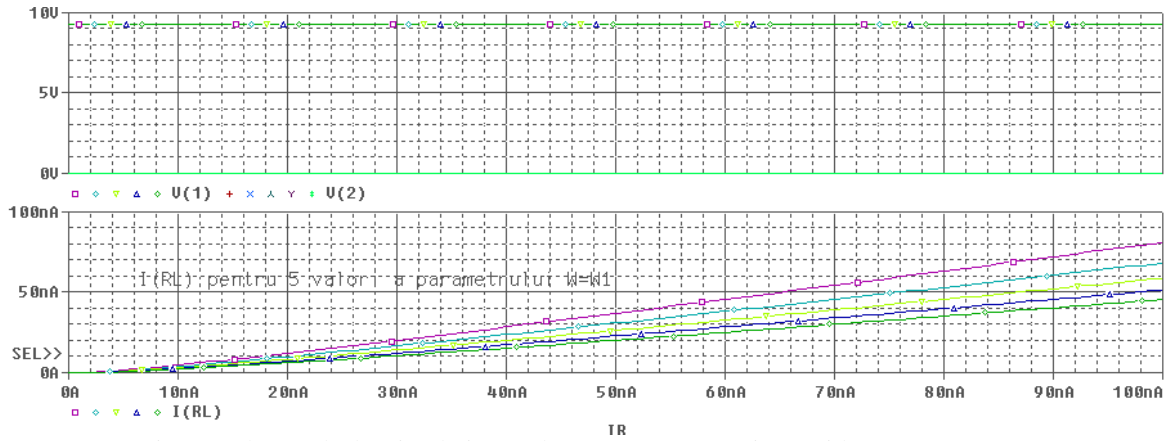


Fig. 6 – The results by simulation to the current source/mirror with p – MOS-FET, for $W_{1,p} = k = 10, 20, 30, 40, 50$ and $W_{2,p} = 30u$.

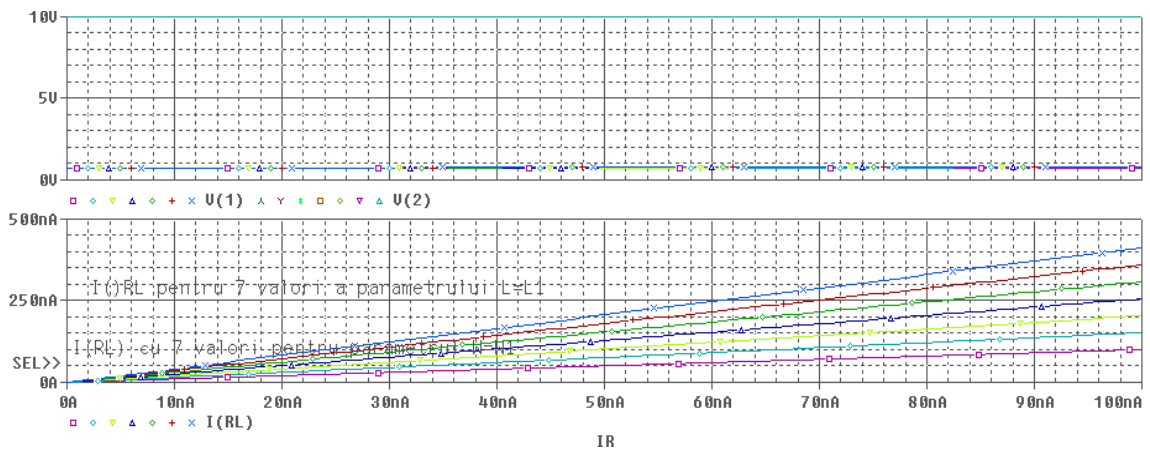


Fig. 7 – The results by simulation to the current source/mirror with n – MOS-FET, for $L_{1,n} = k = 10, 15, 20, 25, 30, 35, 40$ and $L_{2,n} = 20u$.

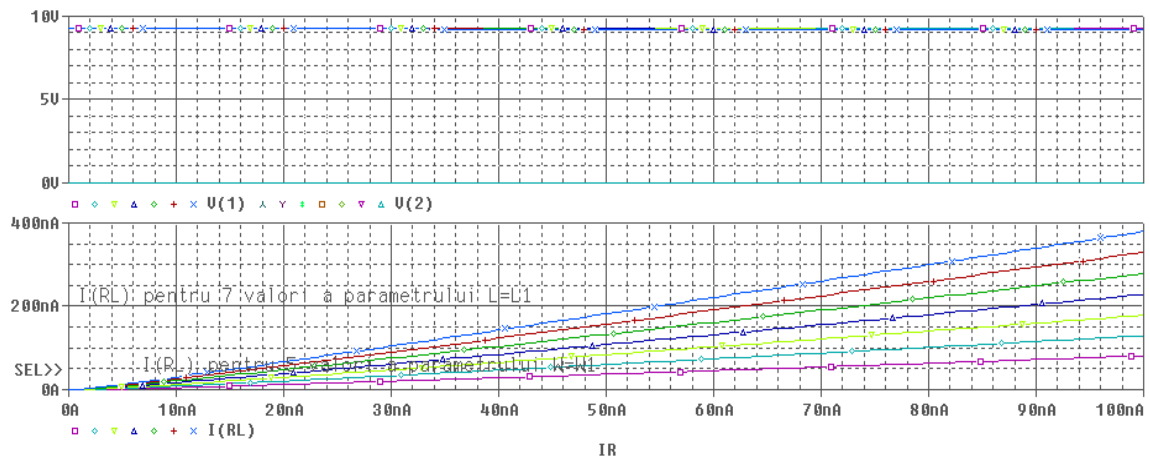


Fig. 8 – The results by simulation to the current source/mirror with p – MOS-FET, for $L_{1,p} = k = 10, 15, 20, 25, 30, 35, 40$ and $L_{2p} = 10u$.

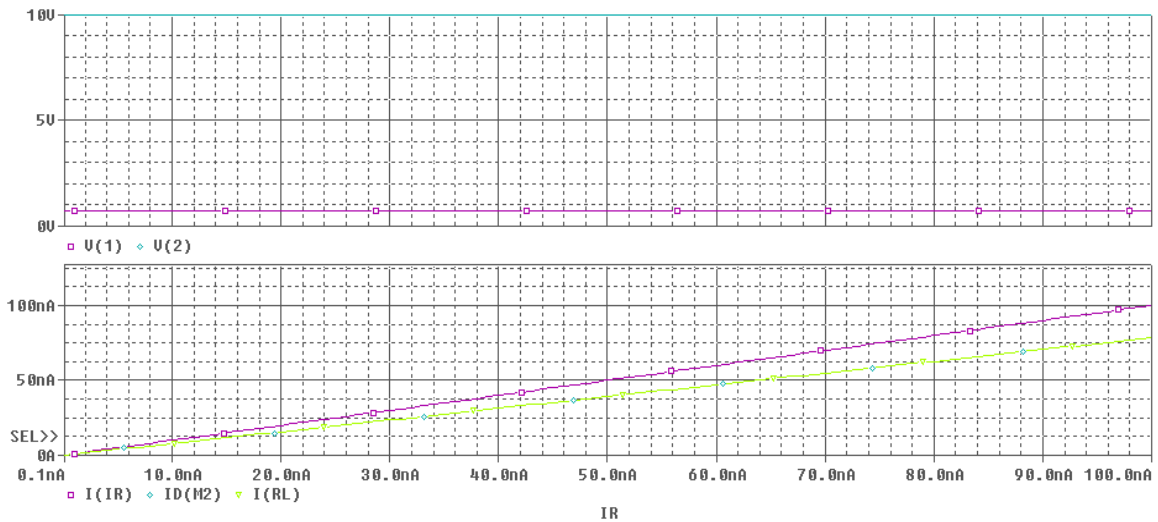


Fig. 9 – The results by simulation to the current source/mirror with n – MOS-FET, for $k_{1,n} = 92.8E-6$ and $k_{2,n} = 72.8E-6$.

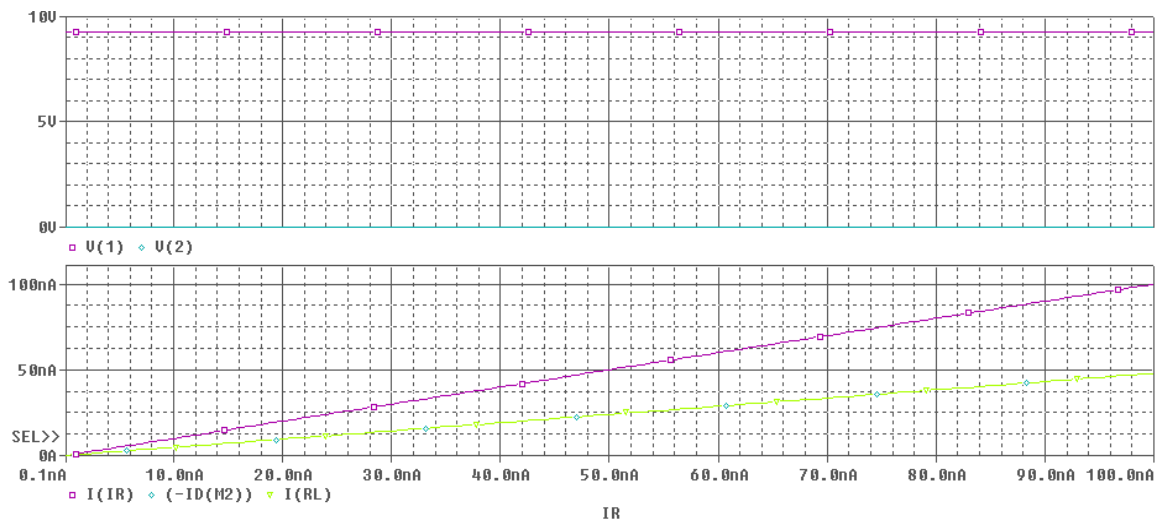


Fig. 10 – The results by simulation to the current source/mirror with p – MOS-FET, for $k_{1,p} = 57.6E-6$ and $k_{2,p} = 27.6E-6$.

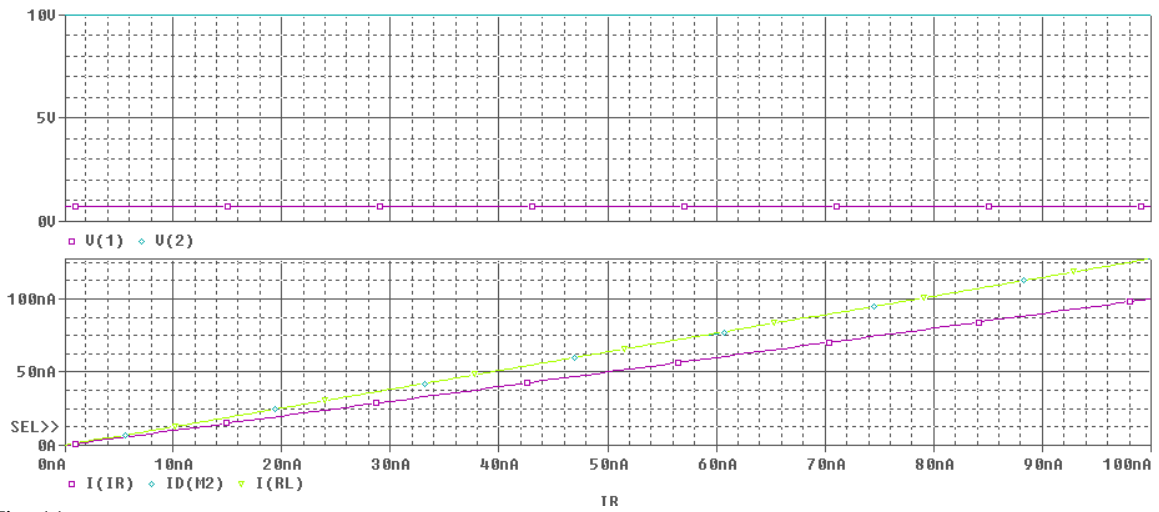


Fig. 11 – The results by simulation to the current source/mirror with n – MOS-FET, for $k_{1,n} = 72.8E-6$ and $k_{2,n} = 92.8E-6$.

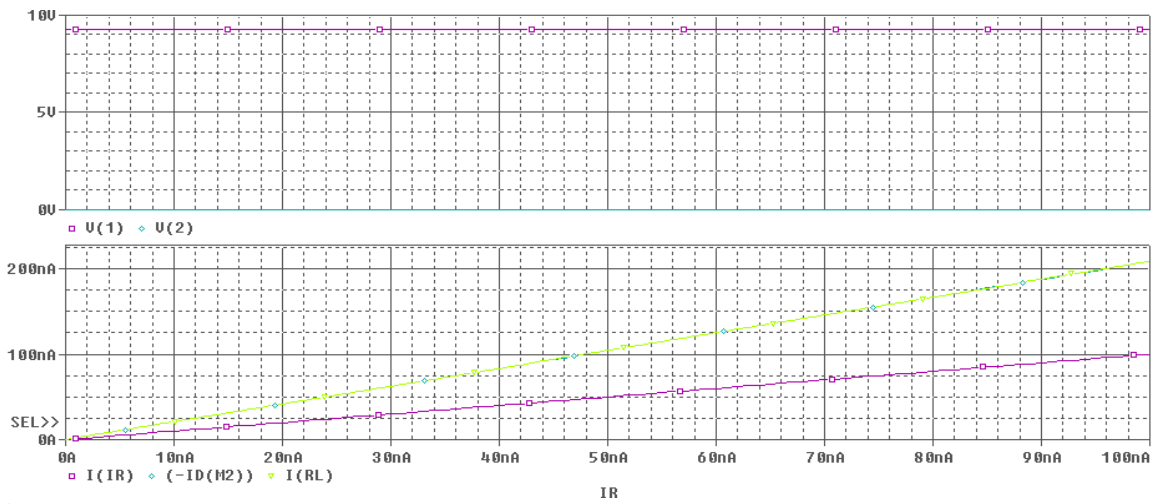


Fig. 12 – The results by simulation to the current source/mirror with p – MOS-FET, for $k_{1,p} = 27.6E-6$ and $k_{2,p} = 57.6E-6$.

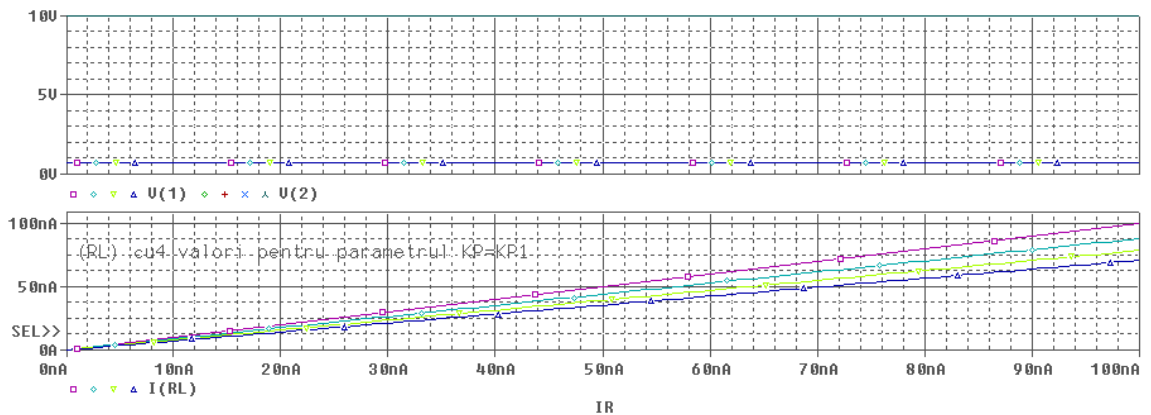


Fig. 13 – The results by simulation to the current source/mirror with n – MOS-FET, for $k_{1,n} = KP_{1,n} = k$ (the parameter with following values: $72.8E-6$, $82.8E-6$, $92.8E-6$, and $102.8E-6$) and $k_{2,n} = KP_{2,n} = 72.8E-6$.

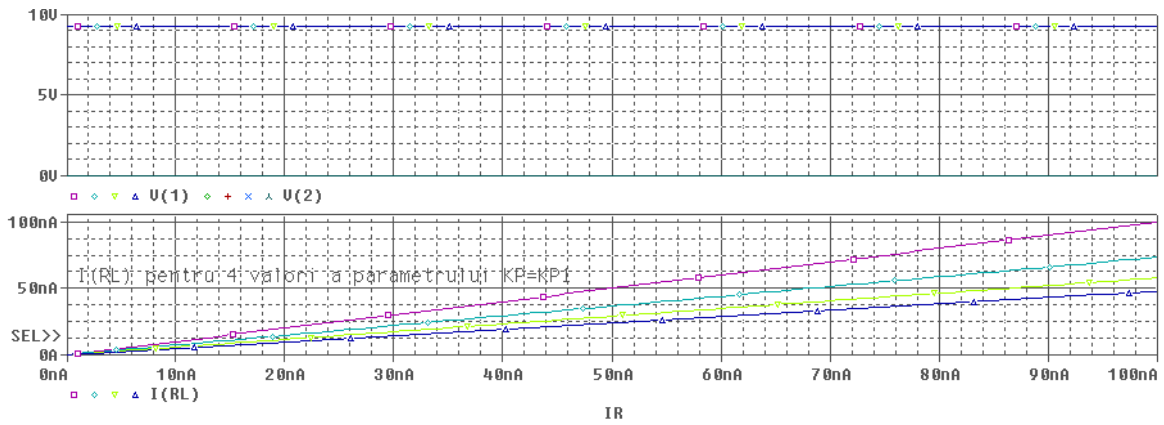


Fig. 14 – The results by simulation to the current source/mirror with p – MOS-FET, for $k_{1,p} = KP_{1,p} = k$ (the parameter with following values: 27.6E-6, 37.6E-6, 47.6E-6, and 57.6E-6) and $k_{2,p} = KP_{2,p} = 27.6E-6$.

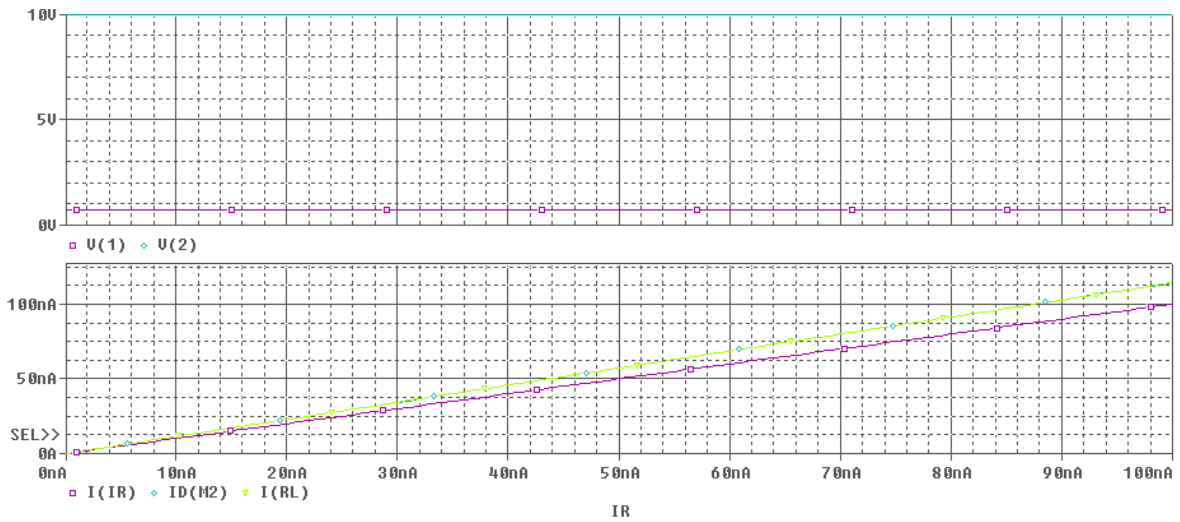


Fig. 15 – The results by simulation to the current source/mirror with n – MOS-FET, for $\gamma_{1,n} = 0.764$ and $\gamma_{2,n} = 0.264$.

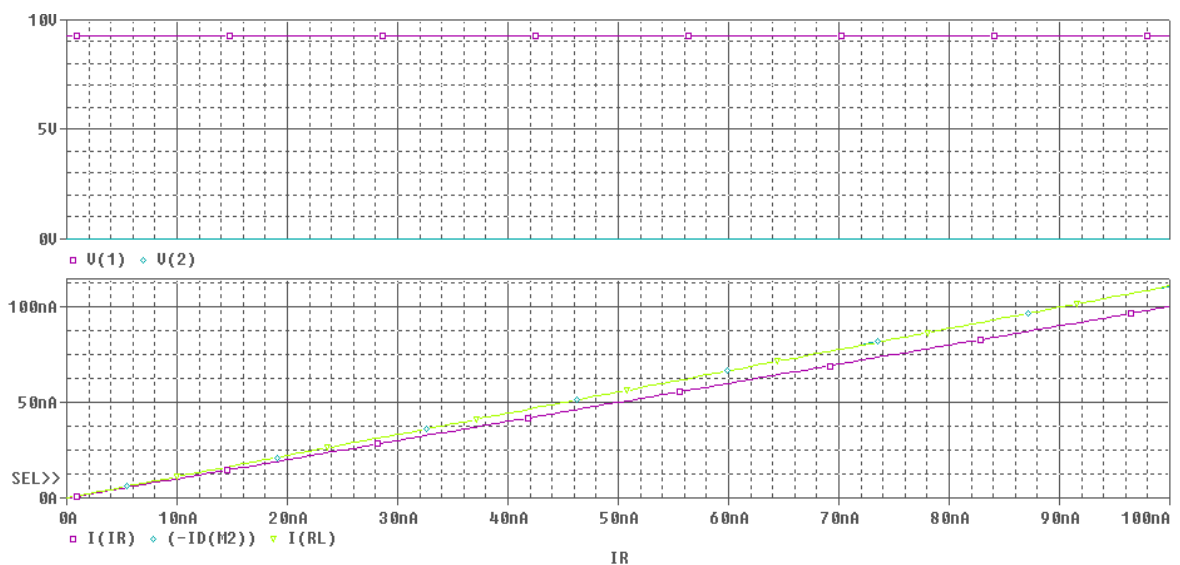


Fig. 16 – The results by simulation to the current source/mirror with p – MOS-FET, for $\gamma_{1,p} = 0.773$ and $\gamma_{2,p} = 0.373$.

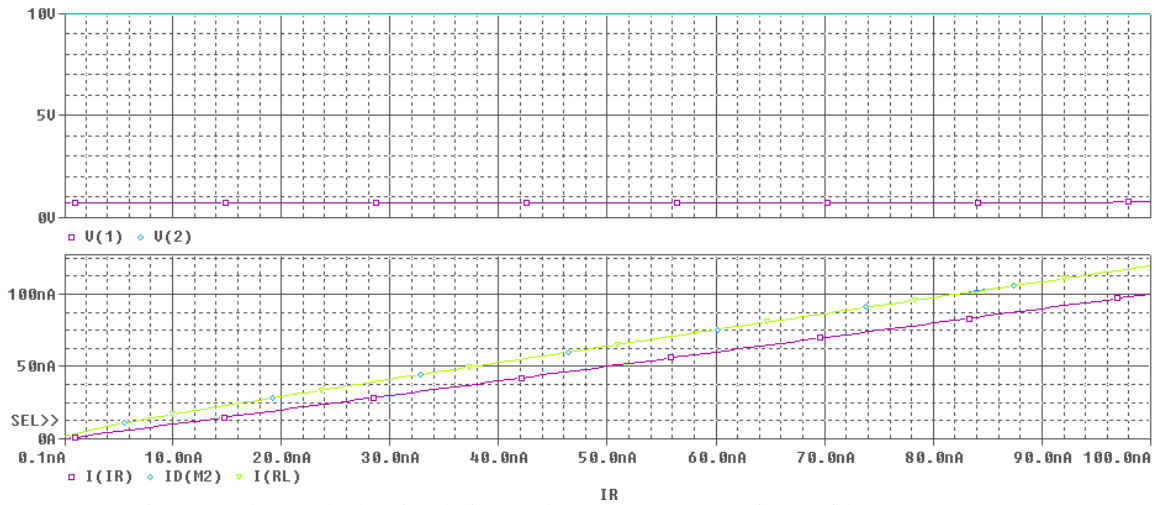


Fig. 17 – The results by simulation to the current source/mirror with n – MOS-FET, for $V_{T0_{1,n}} = 0.705$ and $V_{T0_{2,n}} = 0.7$.

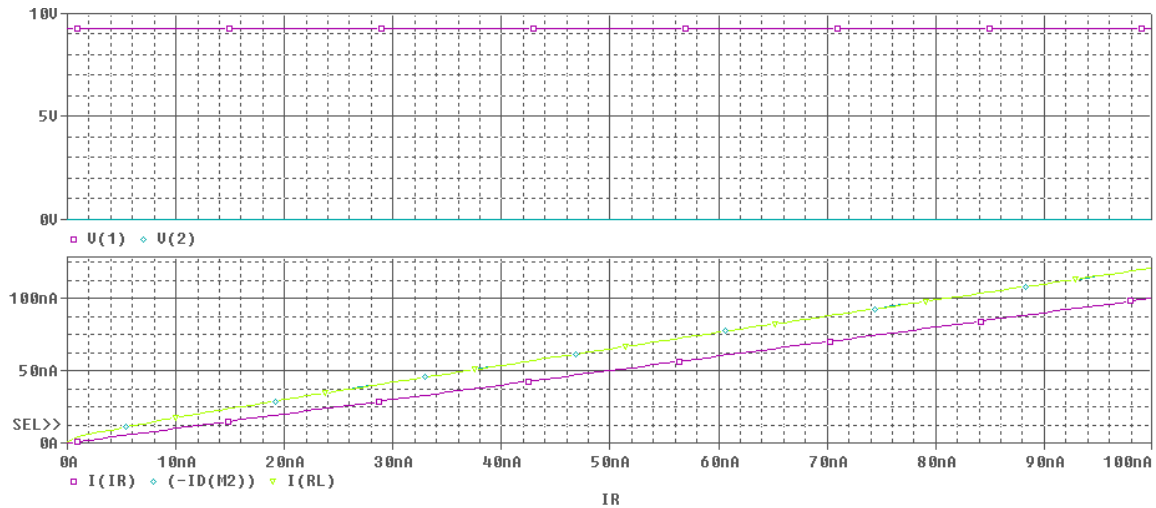


Fig. 18 – The results by simulation to the current source/mirror with p – MOS-FET, for $V_{T0_{1,p}} = -0.705$ and $V_{T0_{2,p}} = -0.7$.

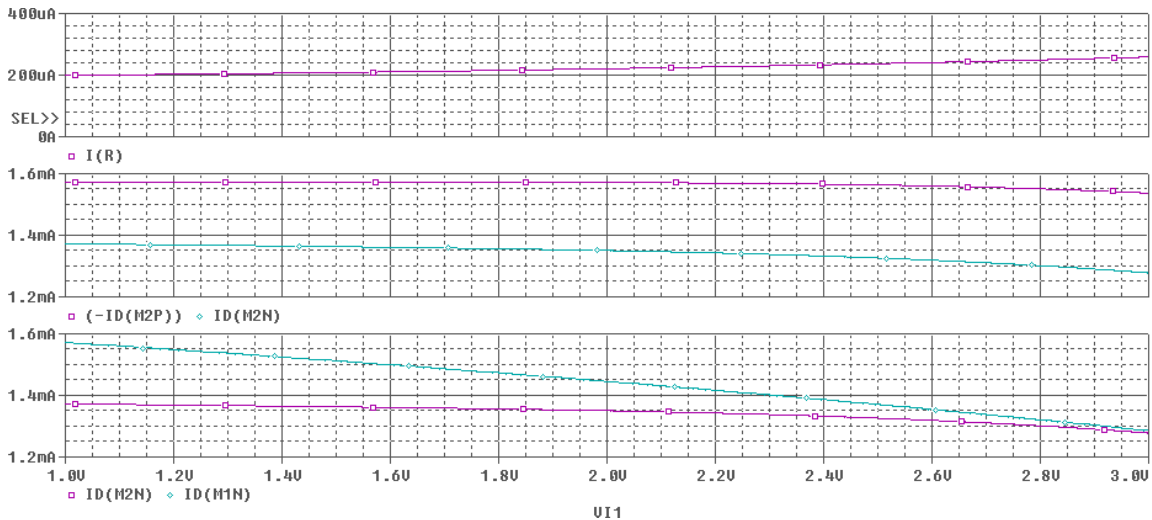


Fig. 19 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$.

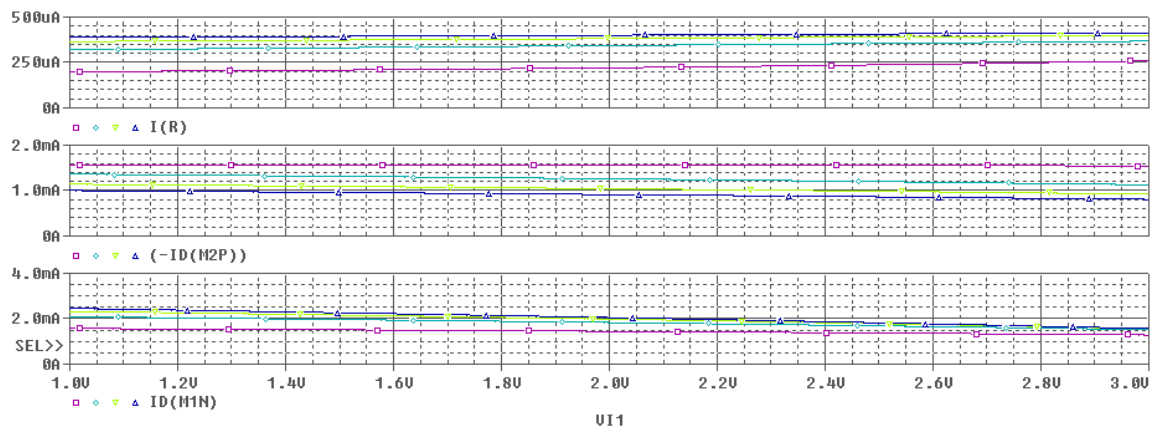


Fig. 20 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $W = W_{l,n} = k = 10, 20, 30, 40$.

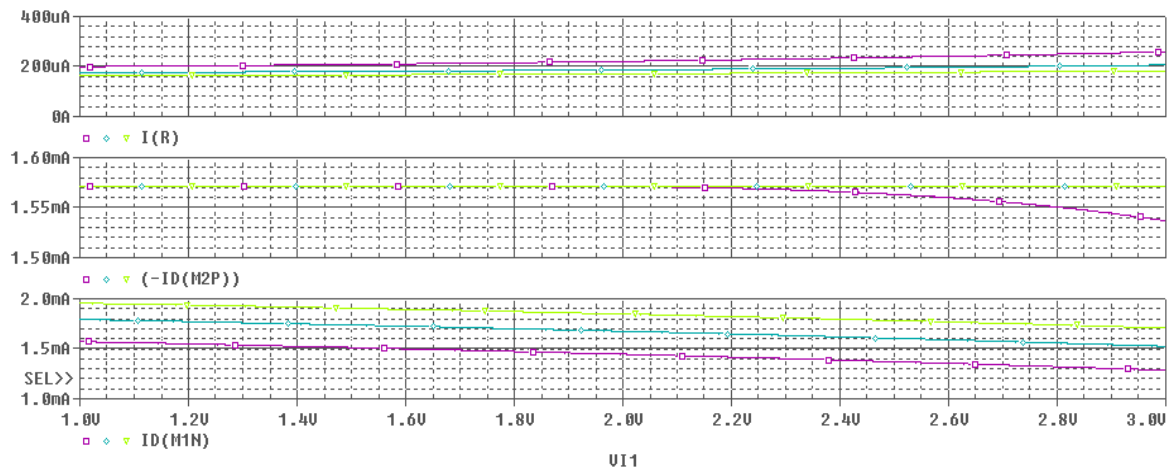


Fig. 21 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $W = W_{l,p} = k = 30, 40, 50$.

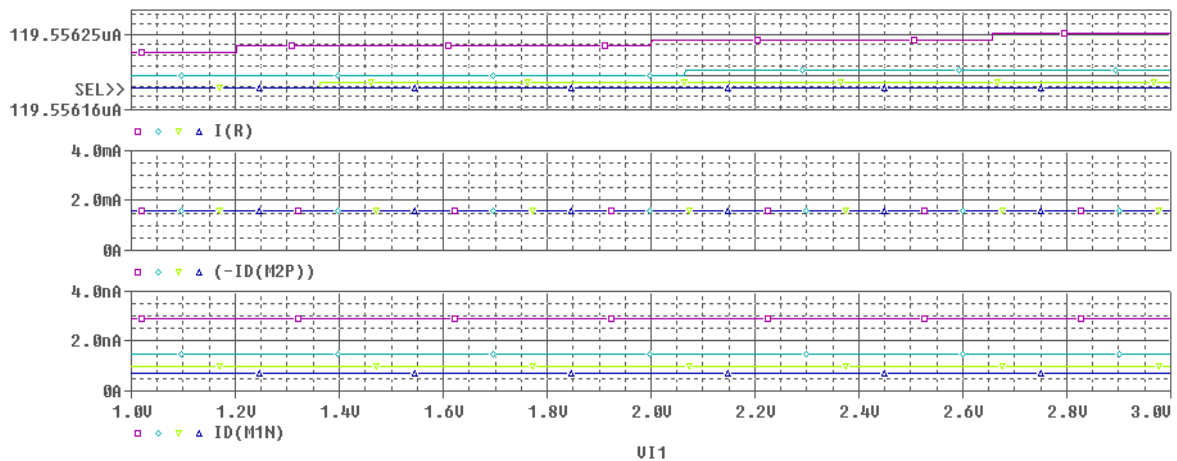


Fig. 22 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $L = L_{l,n} = k = 10, 20, 30, 40$.

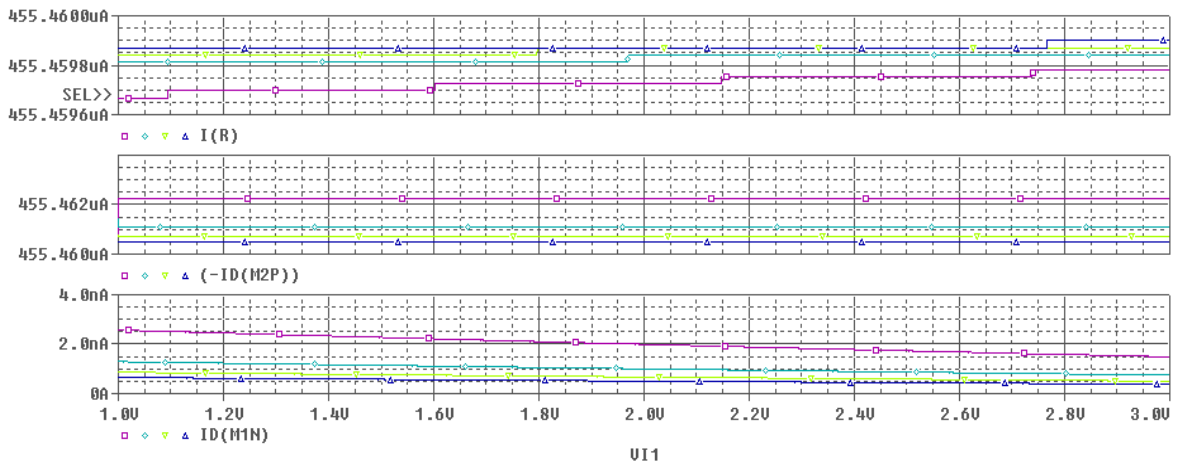


Fig. 23 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $L=L_{1,p} = k = 10, 20, 30, 40$.

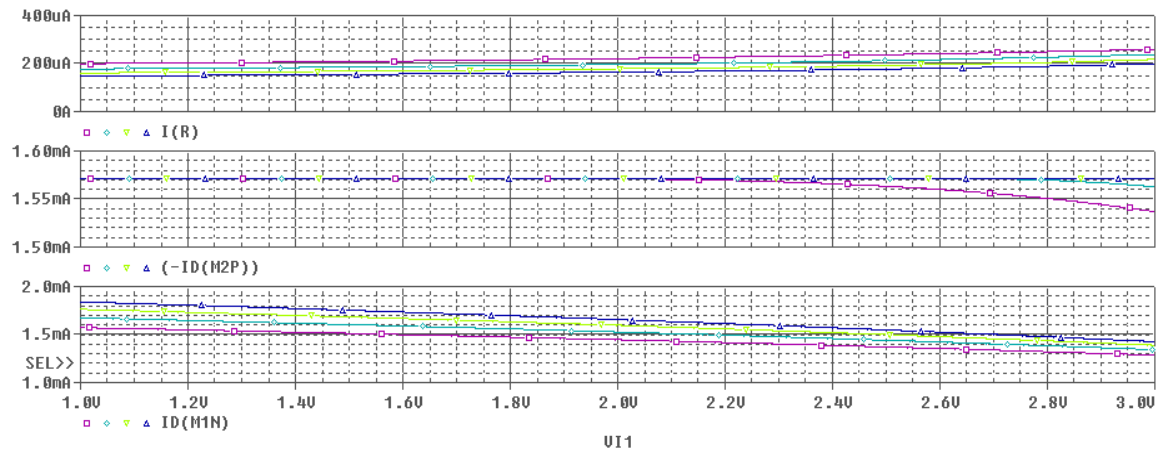


Fig. 24 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $k=KP_{1,n} = k = 72.8\text{E-}6, 82.8\text{E-}6, 92.8\text{E-}6, 102.8\text{E-}6$.

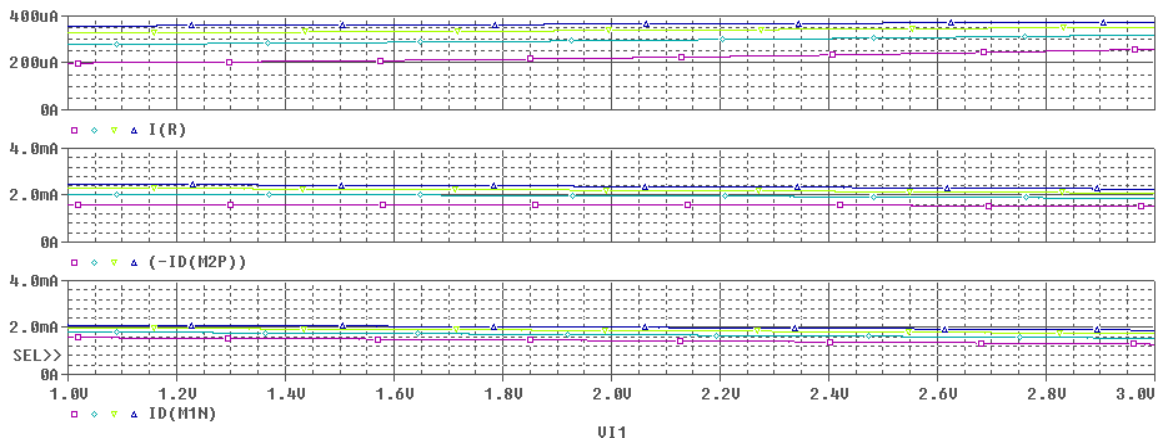


Fig. 25 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $k=KP_{1,n} = k = 27.6\text{E-}6, 37.6\text{E-}6, 47.6\text{E-}6, 57.6\text{E-}6$.

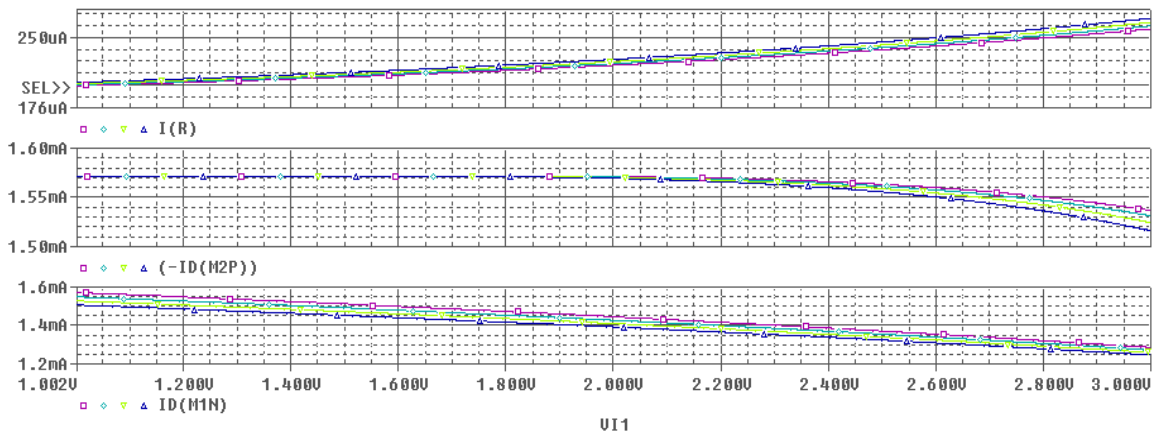


Fig. 26 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $\gamma_{1,n} = k = 0.264, 0.364, 0.464, 0.564$.

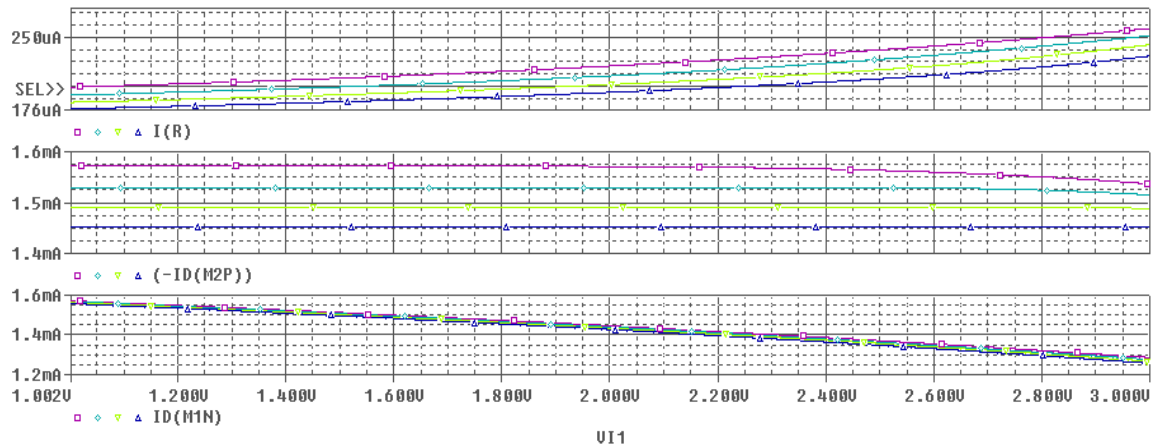


Fig. 27 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $\gamma_{1,p} = k = 0.373, 0.473, 0.573, 0.673$.

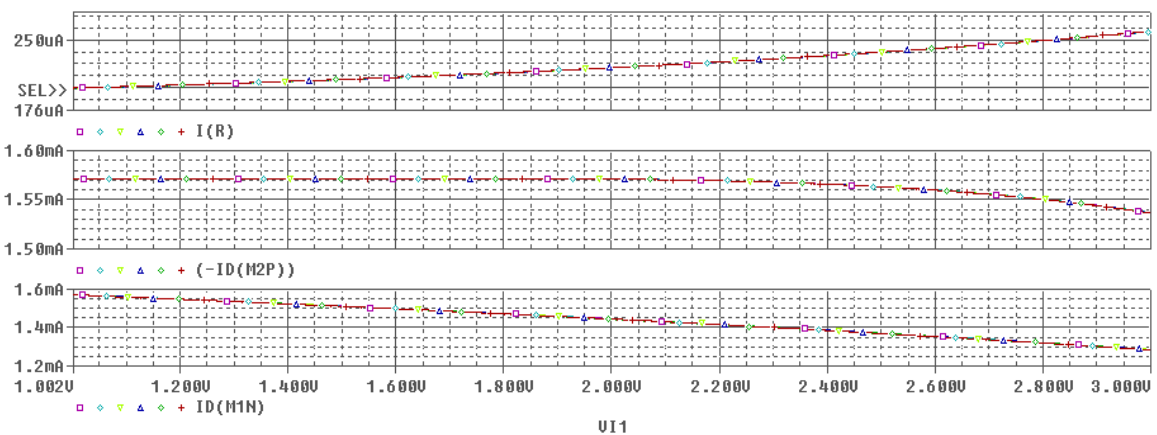


Fig. 28 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $V_{T0} = V_{T0,1,n} = k = 0.700, 0.701, 0.702, 0.703, 0.704, 0.705$.

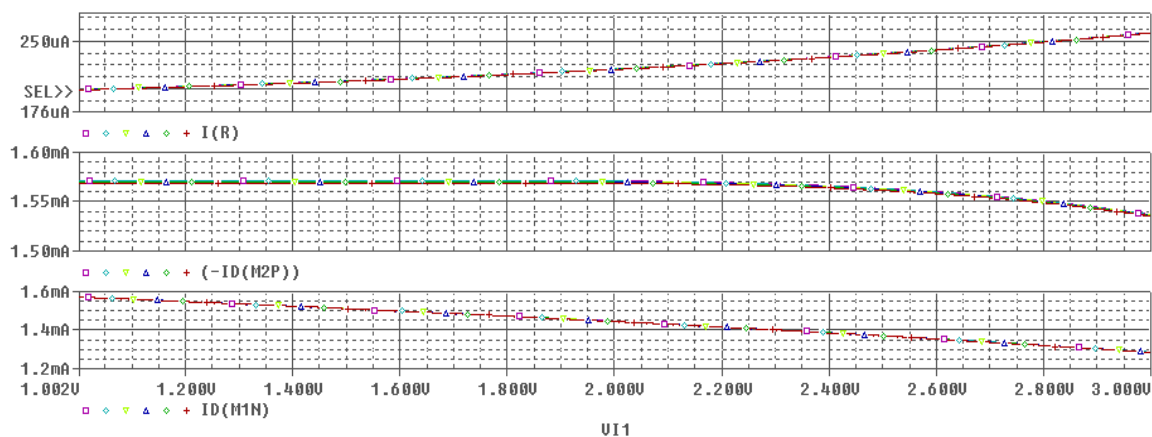


Fig. 29 – The results by simulation to the CMOS fuzzy logic gate of MAX with $R = 20 \text{ k}\Omega$ and $V_{T0} = V_{T0I,p} = k = -0.700, -0.701, -0.702, -0.703, -0.704, -0.705$.

The technological parameters are referred with the following values:

M1 11 0 0 nm1 L=10u W=10u AD=60p AS=60p PD=22u PS=22u

M2 2 1 0 0 nm2 L=10u W=10u AD=60p AS=60p PD=22u PS=22u

where M1 and M2 devices are defined by the following models:

```
.MODEL nm1 nmos(LEVEL=3 VTO=+.7 KP=72.8E-6 GAMMA=.264
+ JS=1.48E-6 PHI=.652 LAMBDA=.0108 PB=.915
+ LD=.2E-6 CGSO=2.76E-10 CGDO=2.76E-10 CGBO=2.76E-10
+ RSH=30 CJ=1.9E-4 MJ=.5 CJSW=1.0E-9
+ MJSW=.5 TOX=250E-10 KF=6.624E-28)
```

```
.MODEL nm2 nmos(LEVEL=3 VTO=+.7 KP=72.8E-6 GAMMA=.264
+ JS=1.48E-6 PHI=.652 LAMBDA=.0108 PB=.915
+ LD=.2E-6 CGSO=2.76E-10 CGDO=2.76E-10 CGBO=2.76E-10
+ RSH=30 CJ=1.9E-4 MJ=.5 CJSW=1.0E-9
+ MJSW=.5 TOX=250E-10 KF=6.624E-28)
```

```
.MODEL pm1 pmos(LEVEL=3 VTO=-.7 KP=27.6E-6 GAMMA=.373
+ JS=4.60E-7 PHI=.688 LAMBDA=.0102 PB=.915
+ LD=.3E-6 CGSO=4.14E-10 CGDO=4.14E-10 CGBO=2.76E-10
+ RSH=40 CJ=2.7E-4 MJ=.5 CJSW=2.0E-9
+ MJSW=.5 TOX=250E-10 KF=1.1E-28)
```

```
.MODEL pm2 pmos(LEVEL=3 VTO=-.7 KP=27.6E-6 GAMMA=.373
+ JS=4.60E-7 PHI=.688 LAMBDA=.0102 PB=.915
+ LD=.3E-6 CGSO=4.14E-10 CGDO=4.14E-10 CGBO=2.76E-10
+ RSH=40 CJ=2.7E-4 MJ=.5 CJSW=2.0E-9
+ MJSW=.5 TOX=250E-10 KF=1.1E-28)
```

The figures presented above show the influence of the relative deviation of the output current versus deviation of the channel width (ΔW), of the channel length (ΔL), of the gain coefficient (Δk), of the body-bias coefficient ($\Delta \gamma$), of the threshold voltage (ΔV_{T0}) and of the supply voltage for the n(p) – MOS-FET current

mirrors (fig. 1) and CMOS fuzzy logic gate of MAX (fig. 2).

The results based on simulation confirm that the sensitivities obtained are in agree well with the values calculated and are caused by deviations the parameters at devices of current mirrors [8].

4. CONCLUSIONS

This paper presents the first method for the evaluation of the current mirrors and of the elementary fuzzy logic gates sensitivities.

From the phenomenological point of view, the sensitivities for the n(p) – MOS-FET current mirrors (fig. 1) and the CMOS fuzzy logic gate of MAX (fig.2) relieve very complex aspects from the above results obtained by simulation in SPICE.

The complex configurations of the CMOS fuzzy logic gates exhibit the distinctive features of the basic n(p) – MOS-FET current mirrors and the elementary CMOS fuzzy logic gate of MAX structure.

5. REFERENCES

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